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     12jun02 08:56:08 User267149 Session D138.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Jun W2
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  File   6:NTIS  1964-2002/Jun W4
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*File   6: See HELP CODES6 for a short list of the Subject Heading Codes
(SC=, SH=) used in NTIS.
  File   8:Ei Compendex(R)  1970-2002/Jun W2
         (c) 2002 Engineering Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Jun W2
         (c) 2002 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2002/May
         (c) 2002 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2002/Jun W2
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  File  77:Conference Papers Index  1973-2002/May
         (c) 2002 Cambridge Sci Abs
  File  94:JICST-EPlus  1985-2002/Apr W3
         (c)2002 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Apr
         (c) 2002 The HW Wilson Co.
  File 108:Aerospace Database  1962-2002/Jun
         (c) 2002 AIAA
  File 144:Pascal  1973-2002/Jun W2
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  File 238:Abs. in New Tech & Eng.  1981-2002/May
         (c) 2002 Reed-Elsevier (UK) Ltd.
  File 305:Analytical Abstracts  1980-2002/May W4
         (c) 2002 Royal Soc Chemistry
*File 305: Frequency of updates and Alerts changing to weekly.
See HELP NEWS 305.
  File 315:ChemEng & Biotec Abs  1970-2001/Dec
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12/06/2002   09/992,387

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Set      Items    Description
S1        6233    (BALL()GRID OR BGA OR LAND()GRID OR PAD()GRID OR PIN()GRID-
                 )(3N)ARRAY? ?
S2        4336    INTERCONNECT??????(3N)DENSIT?????
S3       92677    100(W)(MU OR MICRON? ?)
S4        4220    (MU OR MICRON? ?)(3N)(CENTER? ? OR CENTR?????)
S5        4244    PITCH???(3N)(MICRON? ? OR MU)
S6         226    PITCH???(2N)CENTER? ?
S7      104835    S2:S6
S8     1476732    SILICON OR SI
S9      434353    INTEGRAT??????(2N)(CIRCUIT??? OR IC)
S10      46254    ACTIVE(3N)SURFACE? ?
S11       3350    PASSIVE(3N)SURFACE? ?
S12       1808    CONTACT????(3N)PAD???
S13    3036735    ELECTRIC???
S14      61641    (COUPL??? OR CONNECT??? OR LINK??? OR JOIN???)(3N) (MEMBER?
                  ? OR UNIT? ? OR PART? ?)
S15      11292    S13 AND S14
S16   12994667    ((THIN()FILM???) OR LAYER??? OR COAT??? OR SUBSTRAT????? OR
                  MATERIAL? ? OR SUBSTANCE? ? OR (UNDERL????(2N)LAYER???) OR B-
                 ASE? ?)
S17     467578    INSULAT?????
S18     259048    S16 AND S17
S19        445    INTERPOSER? ?
S20     632676    POLYIMIDE? ? OR POLYIMIDO OR RESIN OR EPOX??? OR (HEAT??? -
                 OR WEAR OR CORROSION???)(4N)RESIST???????
S21      10784    IMIDO OR IMIDE???(2N)POLYMER???
S22     637690    S20:S21
S23       8874    WIRE? ?(2N)(BOND??? OR BALL? ?)
S24       8580    (SOLDER??? OR FUSIBLE(2N)ALLOY? ? OR BOND???? OR JOIN??????
                  OR CEMENT????)(5N)(BALL? ? OR BUMP? ?)
S25       1396    (COPPER OR CU)(5N)(BALL? ? OR BUMP? ?)
S26       1159    (NICKEL OR NI)(5N)(BALL? ? OR BUMP? ?)
S27        142    (PALLADIUM OR PD)(5N)(BALL? ? OR BUMP? ?)
S28          1    S25 AND S26 AND S27
S29        135    S25 AND S26
S30      18644    TAPE()AUTOMAT???(1N)BOND??? OR TAB
S31      13402    FLIP()CHIP OR FLIP()BOND
S32      34448    THERMOSETTING? ? OR THERMOPLASTIC???(3N)(BLEND??? OR MIX OR
                  MIXTURE OR MIXING)
S33      33601    THERMO()COMPRESSION??? OR THERMOCOMPRESSION??? OR INTERDIF-
                 FUSION??? OR INTER()DIFFUSION???
S34      86071    ENCAPSULAT?????? OR CAPSULAT??????
S35         10    CI=(CU SS(S)NI SS(S)PD SS)(S)NE=3
S36        145    S35,S29
S37        570    S1 AND S34
S38         26    S37 AND S7
S39          0    S38 AND S36
S40          1    S38 AND S18
S41          0    S38 AND S19
S42          2    S38 AND S22
S43          1    S42 NOT S40
S44          2    S38 AND S23
S45          1    S44 NOT S40,S43
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S46	1	S38 AND S25
S47	1	S46 NOT S45
S48	0	S38 AND S26
S49	0	S38 AND S27
S50	0	S38 AND (S32 OR S33)
S51	68018	S9 AND S8
S52	64	S51 AND (S10 OR S11)
S53	0	S52 AND S15
S54	0	S52 AND S19
S55	3	S52 AND S22
S56	3	S55 NOT S45,S47
S57	0	S52 AND S23
S58	3	S52 AND S7
S59	3	S58 NOT S56
S60	220	S2 AND S1
S61	133	S60 AND S9
S62	3	S61 AND S18
S63	3	S62 NOT S59
S64	3	S61 AND S19
S65	2	S64 NOT S63
S66	880	S20 AND (S24 OR S25 OR S26 OR S27)
S67	426	S66 AND S31
S68	112	S67 AND S34
S69	23	S68 AND S23
S70	6	S69 AND S18
S71	6	S70 NOT S65,S63
S72	570	S1 AND S34
S73	1	S72 AND S14
S74	1	S72 AND S10
S75	1	S74 NOT S73
S76	0	S72 AND S11
S77	2	S72 AND S12
S78	1315	S3 AND S9
S79	126	S78 AND S5
S80	33	S79 AND S31
S81	0	S80 AND S36
S82	2	S80 AND S25
S83	4	S80 AND S26
S84	3	RD (unique items)
S85	3	S84 NOT S82
S86	1	S80 AND S27
S87	1	S86 NOT S85
S88	9	S80 AND S22
S89	7	RD (unique items)
S90	295	S9 AND S15
S91	23	S90 AND S8
S92	0	S91 AND S34
S93	1	S91 AND S31
S94	77	S24 AND S19
S95	0	S77 AND S10
S96	0	S77 AND S7
S97	1	S77 AND S22
S98	68	S23 AND S15
S99	2	S98 AND S18
S100	536	S34 AND S24

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S101	22	S100 AND S17
S102	2	S101 AND (S25 OR S26 OR S27 OR S36)

12/06/2002 09/992,387

40/3,AB/1 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15301904 PASCAL No.: 01-0475147
Cyanate-bismaleimide-epoxy resin compositions for flip chip, BGA and CSP pre-**encapsulation**
High-**density interconnect** and systems packaging : Santa Clara CA, 17-20 April 2001
LEE Y Joon; LENOS Howard A; BURRESS Robert V; CAPOTE M Albert
Aguila Technologies, Inc. 310 Via Vera Cruz, Suite 107, San Marcos, CA 92069, United States
International Society for Optical Engineering, Bellingham WA, United States; International Microelectronics and Packaging Society, United States
International conference on high-density interconnect and systems packaging (Santa Clara CA USA) 2001-04-17
Journal: SPIE proceedings series, 2001, 4428 76-81
Language: English
In wafer-level and panel-level fabrication of array devices, such as flip chips and **ball grid arrays** , it is possible to apply underfill encapsulants prior to sawing or dicing. The ideal encapsulant is one that can be applied easily, through screen-printing or lamination of B-staged resins, and also exhibits compatible properties. A high-performance packaging encapsulant was developed using cyanate ester-bismaleimide-epoxy (CBE) resins and a novel crosslinking agent 2-(2-Allyl-phenoxymethyl)-oxirane. Molecular design, filler formulation, curing, and characterizations were conducted to develop the most desirable CBE resin properties for underfill pre-**encapsulation** of wafers and BGA **substrates** . The formulation of a solventless resin composition with low viscosity has been completed and the curing conditions were optimized to minimize intermetallic formation in bumped arrays during cure. An ideal filler formulation was achieved to reduce coefficients of thermal expansion (CTE) without adversely affecting viscosity of the resin. The filled resin exhibited high adhesive strength to different surfaces (organic and inorganic), good thermal stability up to 300 Degree C, a wide range of excellent thermo-mechanical properties (modulus and glass transition temperature), low dielectric constants, CTE values down to 25 ppm/ Degree C, outstanding moisture and chemical resistance, and low ionic residues leading to high volume and surface **insulation** resistance. The screen-printing performance of the filled CBE resins was excellent and a method for creating B-staged laminate films was also demonstrated. A composition was perfected for laser drilling of microvias. The novel, hybrid CBE resins are good candidates for making printed circuit laminates, component encapsulants, and solder masks for high-density electronic products.

43/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6392406 INSPEC Abstract Number: B1999-12-0170J-070
Title: Area-array interconnection using Stud-Bump-Bonding
Author(s): Ono, M.; Shiraishi, T.; Bessho, Y.; Eda, K.; Ishida, T.
Author Affiliation: Matsushita Electr. Ind. Co. Ltd., Osaka, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3582 p.893-8
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3582L.893:AAIU;1-9
Material Identity Number: C574-1999-173
Conference Title: 1998 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS
Conference Date: 1-4 Nov. 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: We have previously developed a flip-chip bonding technique, named the Stud-Bump-Bonding (SBB/sup TM/) technique, which can mount bare LSI chips directly on ceramic (MCM-C) and organic substrates (MCM-L). Au bumps are formed on the electrode pads of the LSI chip by wire-bonding apparatus. Each Au bump has two-stepped construction and is bonded with conductive adhesive to an electrode terminal formed on the substrate. An **epoxy** underfill **resin** is inserted to fill the gap between each LSI chip and the substrate. However, it has been supposed that the Stud-Bump-Bonding technique using the wire bonding method was not suitable for area-array interconnection technology, because the bump formation process would damage active devices. We studied the damage to active devices such as MOSFETs and SRAMs caused by wire bonding, leveling of the bumps and mounting. It was found that SBB can be applied to active devices by optimizing the equipment, bonding conditions and materials. Area-array **interconnection** makes high **density interconnection** and LSI chip size reduction possible.

45/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6777149 INSPEC Abstract Number: B2001-01-0170J-069
Title: Assessment of liquid **encapsulated** and transfer molded wirebonded cavity filled packages
Author(s): Ryan, L.; Lynch, B.; Babiarz, A.J.
Author Affiliation: Electron. Mater. Div., Dexter Corp., City of Industry, CA, USA
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.275-80
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2000 Country of Publication: USA 423 pp.
Material Identity Number: XX-2000-01481
Conference Title: Proceedings of Fifth Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: GPD
Conference Date: 25-27 Jan. 2000 Conference Location: Maui, HI, USA
Language: English
Abstract: Thermally enhanced PBGAs are typically cavity down and wirebonded. The majority of heat is extracted through the back of the die which is attached with a conductive adhesive to a metal heat sink. These packages are designed for heat dissipation on high power or high-speed chips. Typical I/O counts of these single or multi-tiered substrates exceed 300. Staggered **wire bond** pads with effective **pitches** down to 45 **mu** m are becoming more common. The encapsulant and **encapsulation** process must be optimized to eliminate voiding or "bridging" of the material over the wires. Nearly all of these packages use a fine filler liquid encapsulant at this time. The materials have been optimized to flow through very fine spaces at atmospheric pressure. Also, various liquid dispensing nozzles and dispense techniques have been developed to further increase production throughput. Packages of this type have been in low volume production for over five years. Liquid encapsulants, dispense processes and equipment have continued to improve as package volumes have increased. As progress is made to increase functionality and speed of devices, thermal problems become more pronounced and the use of these packages increases. High volume suppliers have gone from 1998 rates of about 300,000 devices per month to better than 1,000,000 per month in 1999. As semiconductor packagers increase production rates on these packages, the alternative of transfer molding these devices becomes more viable. This paper addresses the advantages and disadvantages of both processes as a function of both total package cost and package reliability.

12/06/2002 09/992,387

47/3,AB/1 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15301764 PASCAL No.: 01-0474984
Vibration fatigue, failure mechanism and reliability of plastic **ball grid array** and plastic quad flat packages
High-**density interconnect** and systems packaging : Santa Clara CA, 17-20 April 2001
LI Ron S; POGLITSCH Larry
Automotive and Industrial Electronics Group, 4000 Commercial Avenue Motorola, Inc., Northbrook, IL 60062, United States
International Society for Optical Engineering, Bellingham WA, United States; International Microelectronics and Packaging Society, United States
International conference on high-density interconnect and systems packaging (Santa Clara CA USA) 2001-04-17
Journal: SPIE proceedings series, 2001, 4428 223-228
Language: English
Replacement of conventional fine pitch leaded devices such as plastic quad flat packages (PQFP) with high I/O count devices such as plastic **ball grid array** packages (PBGA) is seen as one of the primary ways to further integration of automotive electronic packaging. One major concern with PBGA packages in automotive environments is the vibration durability of the solder ball connections associated with their strength and flexibility. This paper addresses PBGA's fatigue capability and reliability issues through experiment tests and numerical analysis. Test method, experimental setup, and analytical approaches are presented. Fatigue endurance of a given component is reported as a function of input vibration excitation level and the location of that component. Observed failure mechanisms of PBGA and PQFP components are further discussed. The experimental results show that the PBGA components have superior fatigue performance than the PQFP components do within typical level of vibration excitation. Test data are then fitted to two-parameter Weibull distributions. Master curves are found for cumulative failure rate for solder **balls** and **copper** leads, respectively. That master curve covers all Weibull distributions of cumulative failure rates at any given vibration excitation levels. Design guidelines addressing fatigue reliability are discussed in terms of printed circuit board layout and application limitations of given components.

12/06/2002 09/992,387

56/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

02479086 INSPEC Abstract Number: A85071687, B85040554
Title: Investigation of mobile ions in **polyimide** films using MPOS structures
Author(s): Zhang, H.K.; Yu, J.; Tang, W.L.
Author Affiliation: Polymere Lab., Shanghai Jiao-Tong Univ., China
Conference Title: 1984 Annual Report of the Conference on Electrical Insulation and Dielectric Phenomena (Cat. No. 84CH1994-3) p.517-22
Publisher: IEEE, New York, NY, USA
Publication Date: 1984 Country of Publication: USA 577 pp.
Conference Sponsor: IEEE
Conference Date: 21-25 Oct. 1984 Conference Location: Claymont, DE, USA
Language: English
Abstract: **Polyimide** (PI) has been widely used in **integrated circuits** and semiconductor devices as a multilevel insulator and **surface-passive** material. Since sodium and other alkali metal ions are the major factors of instability in semiconductor devices, the migratory characteristics of sodium ions in PI have aroused interest among researcher. Unfortunately, at higher temperatures the electronic conductivity in PI increases rapidly, so that the ionic and electronic currents cannot be effectively separated in conventional metal-PI-metal (MPM) structures. In this respect, the metal-PI-SiO/sub 2/-**silicon** (MPOS) structures have proved to work satisfactorily. The thermally stimulated ionic current (TSIC) and the triangular voltage sweep (TVS) techniques are effective methods for investigating the dynamic behaviour of mobile ions in insulating solid materials. Results of TSIC and TVS curves of MPOS samples are shown and the mobility of sodium ions in PI is discussed.

56/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

00027225 INSPEC Abstract Number: B69007457
Title: Thermal impedance of ceramic packages using beam-lead IC chips
Author(s): Hardwick, N.E.
Author Affiliation: Bell Telephone Lab., Allentown, PA, USA
Conference Title: International electron devices meeting p.82
Publisher: IEEE, New York, NY, USA
Publication Date: 1968 Country of Publication: USA 153 pp.
Conference Sponsor: IEEE Electron Devices Group
Conference Date: 23-25 Oct. 1968 Conference Location: Washington, DC, USA
Language: English
Abstract: Abstract only given, substantially as follows: An **integrated circuit** package utilizing beam-lead sealed junction (BLSJ) **silicon** chips either singly or in multiple arrays consists of a ceramic (99.5% Al/sub 2/O/sub 3/) substrate with a thin film metallic conductor pattern. The beam-leaded chip (or chips) is thermocompression bonded to the metallizing pattern and coated with a **silicon resin** for protection from humidity and surface contamination. External leads are also TC bonded to the metallizing pattern for connection to the outside world. This paper presents and discusses the results of a three-dimensional analytical approximation of the thermal resistance of a single chip package configuration obtained by calculating the thermal resistance of the individual elements and solving by the electrothermal analog technique. Thermal resistance values are presented for the cases of external leads heat-sinked and the ceramic base heat-sinked with both a centrally located 0.005 in. diameter junction area and a junction evenly distributed over the **active surface** of the chip

56/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02089132
E.I. Monthly No: EIM8605-027432
Title: INVESTIGATION OF MOBILE IONS IN **POLYIMIDE** FILMS USING MPOS STRUCTURES.
Author: Zhang, H. K.; Yu, J.; Tang, W. L.
Corporate Source: Shanghai Jiao-Tong Univ, Polymer Lab, Shanghai, China
Conference Title: 1984 Annual Report - Conference on Electrical Insulation and Dielectric Phenomena.
Conference Location: Wilmington, DE, USA Conference Date: 19841021
E.I. Conference No.: 05822
Source: Annual Report - Conference on Electrical Insulation and Dielectric Phenomena 1984. Publ by IEEE, New York, NY, USA. Available from IEEE Service Cent (Cat n 84CH1994-3), Piscataway, NJ, USA p 517-522
Publication Year: 1984
CODEN: CEIPAZ ISSN: 0084-9162
Language: English
Abstract: **Polyimide** (PI) has been widely used in **integrated circuits** and semiconductor devices as a multilevel insulator and **surface-passive** material. Since sodium and other alkali metal ions are the major factors of instability in semiconductor devices, the migratory characteristics of sodium ions in PI have aroused interest among researchers. Unfortunately, at higher temperatures the electronic conductivity in PI increases rapidly, so that the ionic and electronic currents cannot be effectively separated in conventional metal-PI-metal (MPM) structures. In this respect, the metal-PI-SiO//2- **silicon** (MPOS) structures have proved to work satisfactorily. The thermally stimulated ionic current (TSIC) and the triangular voltage sweep (TVS) techniques are effective methods for investigating the dynamic behavior of mobile ions in insulating solid materials. Results of TSIC and TVS curves of MPOS samples are shown and the mobility of sodium ions in PI is discussed. 5 refs.

12/06/2002 09/992,387

59/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5567886 INSPEC Abstract Number: B9706-1265D-011
Title: A high performance 0.25 mu m CMOS technology for fast SRAMs
Author(s): Hayden, J.D.; McNelly, T.F.; Perera, A.H.; Pfiester, J.R.; Subramanian, C.K.; Thompson, M.A.
Author Affiliation: Adv. Products Res. & Dev. Lab., Motorola Inc., Austin, TX, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2875 p.148-63
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1996 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1996)2875L.148:HP2C;1-M
Material Identity Number: C574-96227
U.S. Copyright Clearance Center Code: 0 8194 2273 8/96/$6.00
Conference Title: Microelectronic Device and Multilevel Interconnection Technology II
Conference Sponsor: SPIE
Conference Date: 16-17 Oct. 1996 Conference Location: Austin, TX, USA
Language: English
Abstract: A high performance 0.25 mu m CMOS process has been developed for fast SRAMs. This technology features retrograde wells, shallow trench isolation scalable to 0.45 **mu** m **active pitch, surface** channel 0.25 mu m NMOS and PMOS transistors with a 55 AA nitrided gate oxide providing drive currents of 630 and 300 mu A/ mu m respectively at off-leakages of 10 pA/ mu m, overgated TFTs with an on/off ratio >6*10/sup 5/, stacked capacitors for improved SER protection, five levels of polysilicon planarized by chemical-mechanical polishing (CMP) with two self-aligned interpoly contacts, 0.35 mu m contacts and a 0.625 metal pitch. A triple well structure was used for SER protection. High energy retrograde wells were integrated with shallow trench isolation and EPI, giving excellent interwell isolation for both leakage and latch-up down to n/sup +//p/sup +/ spaces of 0.60 mu m. PMOS transistors were scaled to 0.1 mu m gate length while maintaining excellent short channel characteristics. A split word-line bitcell was scaled to 1.425 mu m*2.625 mu m=3.74 mu m/sup 2/ using 0.25 mu m rules. A W interpoly plug connected PMOS TFT loads to underlying NMOS latch gates without a parasitic diode or dopant interdiffusion, connecting 3 polysilicon layers with self-aligned isolation from an intervening polysilicon layer used as a local interconnect. TFT drive currents were improved by the plug, particularly at low voltages and the memory nodes pulled to the full supply voltage. Functional 0.25 mu m bitcells were demonstrated and with an LDD resistor cell, stability could be doubled. Bitcell simulation showed that a 4T bitcell is stable at 2.5 V but that a word-fine boost is required for 1.8 V operation.

59/3,AB/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04601695
E.I. No: EIP96103370393
Title: High-performance 0.25-um CMOS technology for fast SRAMs
Author: Hayden, James D.; McNelly, T.F.; Perera, A.H.; Pfiester, J.R.; Subramanian, C.K.; Thompson, Matthew A.
Corporate Source: Motorola, Austin, TX, USA
Conference Title: Microelectronic Device and Multilevel Interconnection Technology II
Conference Location: Austin, TX, USA Conference Date: 19961016-19961017
E.I. Conference No.: 22640
Source: Proceedings of SPIE - The International Society for Optical Engineering v 2875 1996.. p 148-163
Publication Year: 1996
CODEN: PSISDG ISBN: 0-8194-2273-8
Language: English
Abstract: A high performance 0.25 mu m CMOS process has been developed for fast static RAMs. This technology features retrograde wells, shallow trench isolation scalable to a 0.45 **mu** m **active pitch, surface** channel 0.25 mu m NMOS and PMOS transistors with a 55 angstroms nitrided gate oxide providing drive currents of 630 and 300 mu A/ mu m respectively at off-leakages of 10 pA/ mu m, overgated TFTs with an on/off ratio greater than 6 center dot 10**5, stacked capacitors for improved SER protection, five levels of polysilicon planarized by chemical-mechanical polishing with two self-aligned interpoly contacts, 0.35 mu m contacts and a 0.625 metal pitch. In this technology, a triple well structure was used for SER protection. High energy retrograde wells were integrated with shallow trench isolation and epi providing excellent interwell isolation for both leakage and latch-up down to n plus /p plus spaces of 0.60 mu m. PMOS transistors were scaled to a physical gate length of 0.1 mu m while maintaining excellent short channel characteristics. A split word-line bitcell was scaled to 1.425 mu m multiplied by 2.625 mu m equals 3.74 mu m**2 using 0.25 mu m rules. A tungsten interpoly plug was used to connect the PMOS TFT loads to the underlying NMOS latch gates without a parasitic diode or dopant interdiffusion, connecting 3 polysilicon layers with self-aligned isolation from an intervening polysilicon layer used as a local interconnect. With this plug, TFT drive currents were greatly improved, particularly at low voltages and the memory nodes pulled to the fully supply voltage. Functional 0.25 mu m bitcells were demonstrated and with an LDD resistor it was possible to double the cell stability. Bitcell simulation was used to demonstrate that a 4T bitcell will be stable at 2.5 V but that a word-line boost will be required for 1.8 V operation. 7 Refs.

12/06/2002 09/992,387

59/3,AB/3 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

07571331 Genuine Article#: 182TB Number of References: 184
Title: The fluid mechanics of microdevices - The Freeman Scholar Lecture (ABSTRACT AVAILABLE)
Author(s): GadelHak M (REPRINT)
Corporate Source: UNIV NOTRE DAME,DEPT AEROSP & MECH ENGN/NOTRE DAME//IN/46556 (REPRINT)
Journal: JOURNAL OF FLUIDS ENGINEERING-TRANSACTIONS OF THE ASME, 1999, V121 , N1 (MAR), P5-33
ISSN: 0098-2202 Publication date: 19990300
Publisher: ASME-AMER SOC MECHANICAL ENG, 345 E 47TH ST, NEW YORK, NY 10017
Language: English Document Type: REVIEW
Abstract: Manufacturing processes that can create extremely small machines have been developed in recent years. Microelectromechanical systems (MEMS) refer to devices that have characteristic length of less than I mm but more than I micron, that combine electrical and mechanical components and that are fabricated using **integrated circuit** batch-processing techniques. Electrostatic, magnetic, pneumatic and thermal actuators, motors, valves, gears, and tweezers of less than **100-mu** m size have been fabricated. These have been used as sensors for pressure, temperature, mass flow, velocity and sound, as actuators for linear and angular motions, and as simple components for complex systems such as micro-heat-engines and micro-hear-pumps, The technology is progressing at a I are that far exceeds that of our understanding of the the unconventional physics involved in the operation as well as the manufacturing of those minute devices. The primary objective of this article is to critically review the status of our understanding of fluid flow phenomena particular to microdevices. In tel-ms of applications, the paper emphasizes the use of MEMS as sensors and actuators for flow diagnosis and control.

63/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6709747 INSPEC Abstract Number: B2000-10-0170J-127, C2000-10-5490-003
Title: High performance package designs for a 1 GHz microprocessor
Author(s): Hasan, A.; Sarangi, A.; Baldwin, C.S.; Sankman, R.L.; Taylor, G.F.
Author Affiliation: Intel Corp., Chandler, AZ, USA
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070) p.1178-84
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xxxv+1756 pp.
ISBN: 0 7803 5908 9 Material Identity Number: XX-2000-01366
U.S. Copyright Clearance Center Code: 0 7803 5908 9/2000/$10.00
Conference Title: 2000 Proceedings. 50th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, and Manuf. Technol. Soc. of IEEE; Electronic Ind. Alliance
Conference Date: 21-24 May 2000 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: This paper describes the architecture and design of an Organic **Land Grid Array** (OLGA) and a Flip Chip **Pin Grid Array** (FCPGA) package for a 32 bit microprocessor with a clock frequency of 1 GHz and an I/O bus designed to run at 133 MHz. Cost and performance targets and compatibility with existing systems are the key accomplishments of this design project. Issues and implementation details of each of these aspects are discussed and contrasted here. There are many items in design which directly or indirectly impact package cost: I/O timings, signal trace impedance, number of routing **layers**, power delivery, thermal performance, and silicon and system level interface, among others. Often, trade-offs need to be made in the design to balance performance and cost. OLGA and FCPGA technologies have differences in package **substrate material**, manufacturing process, and platform interface. The OLGA package has a 4-**layer** organic laminated **substrate**, copper conductors, low dielectric constant **insulators**, high **density interconnect** rules for routing and silicon connectivity, and surface mounting capability for the system interface. The FCPGA package, a 6-**layer** laminated printed circuit board with blind microvias and buried, plated through hole (PTH) vias, has a relaxed set of interconnect and routing rules, and enables direct socketability for system interface. This paper concentrates on the processor performance issues associated with the package routing and power delivery. Due to high inductance associated with the socket and package pins in the FCPGA package, power supply loop inductance was a concern for high frequency power delivery. To overcome this problem, a certain number of decoupling capacitors were placed on the underside of the package **substrate** . This paper discusses an optimal placement scheme for the capacitors and their effectiveness in performance improvement of the system compared to the OLGA package case.

12/06/2002 09/992,387

63/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6351723 INSPEC Abstract Number: B1999-10-0170J-068
Title: New build-up printed wiring board for flip chip attach **based** on unique high T/sub g/ epoxy resin
Author(s): Fujiwara, H.; Esaki, Y.
Author Affiliation: Matsushita Electr. Works Ltd., Osaka, Japan
Conference Title: Fifth Annual National Symposium. Emerging Technologies. Proceedings of the Technical Program p.17-22
Publisher: SMTA, Edina, MA, USA
Publication Date: 1998 Country of Publication: USA 159 pp.
Material Identity Number: XX-1998-03540
Conference Title: Proceedings of New and Emerging Technologies for Surface Mounted Electronic Packaging
Conference Date: 16-18 Nov. 1998 Conference Location: Chandler, AZ, USA
Language: English
Abstract: We have developed a new technology for build-up printed wiring board (PWB) fabrication for application to flip chip attachment (FCA). The build-up **layers** consist of a thin **coating** of high T/sub g/ thermosetting epoxy resin, developed for the heat-resistant PWB. Use of this **material** makes the thin **layers** maintain high heat-resistance (T/sub g/=180 degrees C corresponding to FR-5 grade) and high **insulation** reliability. It is currently too difficult to maintain these characteristics if a photo-sensitive resin process is used for the PWB, as such resins typically use the general epoxy acrylate resin, including hydrophoric functions. The build-up PWB has very small interstitial blind via holes (IVH) with 80 mu m minimum diameter produced by a pulse oscillated CO/sub 2/ laser. These IVH can condense the signal traces and provide a circuit design with more flexibility. Moreover, they can achieve finer patterns (e.g. L/S=20/20 mu m) than the previous subtractive process. The tighter pattern alignment tolerance (+or-25 mu m or less) is also practical with the combination of the semi-additive process and a high-performance exposure unit. These processes and techniques can be useful for making a build-up PWB IC package which performs as an interposer between semiconductor and motherboard. At present, ICs tend to be more densely integrated and require higher **density interconnect** solutions. This new build-up PWB is a better solution for advanced assembly technology: FCA, **BGA** (**ball grid array**), CSP (chip scale packages), etc. In this paper, we focus on the unique high T/sub g/ epoxy resin system with detailed **materials** and reliability data.

63/3,AB/3 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04672377 JICST ACCESSION NUMBER: 00A0808289 FILE SEGMENT: JICST-E
Electronic **Materials** for High Density Packaging Technologies.
Technical Trend of Multilayer **Materials** for Printed Wiring Boards.
TAKATA TOSHIHARU (1); AKAMATSU MOTOYUKI (2); SAITO EIICHIRO (2); MATSUSHITA YUKIO (2)
(1) Matsushita Electr. Work., Ltd.; (2) Matsushitadenko Denshizairyor&dse
Matsushita Denko Giho(MEW Technical Report), 2000, NO.71, PAGE.4-8, FIG.7, TBL.5, REF.8
JOURNAL NUMBER: S0151AAP ISSN NO: 0285-5054
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The need to make the electronic equipment multi-functional and smaller has drastically changed the printed wiring boards in their ever expanding global market. Up-graded LSI, compact and higher functional package such as CSP/BGA (Chip Scale/Size Package)/(**Ball Grid Array**) and changes in the mounting technology have required "Build-up PWB" to achieve HDI (High **Density Interconnection**) that is expanding rapidly. This paper explains characteristics of future PWB **materials** required from the trend of LSI package and PWB design, and introduces products and technologies that will be newly developed. (author abst.)

65/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7106415 INSPEC Abstract Number: B2002-01-7630D-012
Title: High density modular packaging for space electronics
Author(s): Massenat, M.R.; Val, A.
Author Affiliation: Matra Marconi Space France, Velizy-Villacoublay, France
Conference Title: Proceedings 2000 HD International Conference on High-Density Interconnect and Systems Packaging (SPIE Vol.4217) p.4-9
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA
Publication Date: 2000 Country of Publication: USA xvi+617 pp.
ISBN: 0 930815 60 2 Material Identity Number: XX-2001-01667
Conference Title: 2000 HD International Conference on High-Density Interconnect and Systems Packaging
Conference Sponsor: SPIE; IMAPS - Int. Microelectron. & Packaging Soc.; CMP Media
Conference Date: 25-28 April 2000 Conference Location: Denver, CO, USA
Language: English
Abstract: While miniaturization and reliability remain fundamental requirements for the design of space electronic equipment, economical aspects are also increasingly driving this industry. Electronic packaging is considered now to be an outstanding factor of competitivity. Matra Marconi Space (MMS) developed a complete set of processes in order to cope with three objectives: (1) smaller, i.e. use of MCM, 3D assembly, grid array SMD packages, high density PCBs; (2) smarter, i.e. more complex functions, higher electrical and thermal performances, high reliability for space environment; and (3) cheaper, i.e. standardization, flexibility, reworkability, testability, high yield automated manufacturing, adaptability to next generation components (nonhermetic technologies), and shorter time-to-market. The best answer to this long list of issues is closely linked to high **density interconnect** use at all packaging levels, beginning with MCM very fine line substrates developed by MMS, followed by high density MCM packaging, 3D **interposers**, specific cooling methods and a modular approach. This allows dismountable highly tolerant electrical, mechanical and thermal assemblies for the different functions inside electronic units, applied to flight computers and processors for space projects currently in development for French and European space agencies and for commercial telecommunication spacecraft.
Subfile: B

65/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5981281 INSPEC Abstract Number: B9809-0170J-012
Title: High density substrates [packaging]
Author(s): Hutton, M.
Journal: Printed Circuit Fabrication vol.21, no.6 p.20-2, 24
Publisher: Miller Freeman,
Publication Date: June 1998 Country of Publication: USA
CODEN: PCFAE6 ISSN: 0274-8096
SICI: 0274-8096(199806)21:6L.20:HDSP;1-G
Material Identity Number: F904-98006
Language: English
Abstract: There is an emerging opportunity for the worldwide advanced PCB industry. Significant investments have been made to develop high **density interconnect** (HDI) boards for portable products such as personal digital assistants (PDA) mobile phones and digital camcorders. A number of companies are developing and using HDI technologies for portable products. However, this technology, developed for portable applications, will be utilized in an emerging new market as an **interposer** for high performance packages. The forecast demand for high performance packages is set to reach nearly five billion units by the year 2006. Typically, these would include microprocessors which can be up to $300 each in value. The initial introduction of lamination technology into IC packaging was to improve the assembly yields of high pin-count PQFPs by using an organic substrate to convert peripheral pins to an area **array** configuration, i.e. **ball grid arrays** (BGAs). As functionality and hence pin-counts have increased, many companies are adopting area array packaging technology, i.e. BGAs, and chip scale packages (CSPs), where solder balls on the base of the **interposer** are used instead of leads for connection of the package to the PCB. Attention is now being focused on the package's construction to improve both electrical performance and reliability while still focusing on cost effectiveness.

12/06/2002 09/992,387

71/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6072083 INSPEC Abstract Number: B9812-2570-015
Title: Low-cost **flip chip** technology for organic **substrates**
Author(s): Baba, S.
Journal: Fujitsu Scientific and Technical Journal vol.34, no.1 p. 78-86
Publisher: Fujitsu,
Publication Date: 1998 Country of Publication: Japan
CODEN: FUSTA4 ISSN: 0016-2523
SICI: 0016-2523(1998)34:1L.78:CFCT;1-6
Material Identity Number: F016-98002
Language: English
Abstract: This paper introduces a **flip chip** technology that is used on various kinds of **substrates** (glass-**epoxy,** flexible printed circuit board, and MCM-L/D). In this technology, Au bumps are formed on the chip I/O pads by **wire bonding** and the **bumps** are pressed onto the **substrate** pads. The chip is bonded and **encapsulated** with a thermosetting adhesive, and conductive paste improves the mechanical and electrical connection between the Au bumps and the **substrate** in order to increase the connection reliability. To apply this technology to different types of **substrates** , we investigated the deformation characteristics of the **substrate** pad and the adhesive strength and **insulation** of the adhesive for **encapsulation** . This technology has been applied to some practical products and reduces the mounting areas of LSI to 1/10 or less that of LSI that use the existing SMD package approach.

12/06/2002 09/992,387

71/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5709566 INSPEC Abstract Number: B9711-0170J-061
Title: Low cost **flip chip** technology for organic **substrates**
Author(s): Baba, S.
Author Affiliation: Fujitsu Labs. Ltd., Kawasaki, Japan
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.268-73
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: This paper describes outline of the **flip chip** technology which is used on various kind of **substrates** (glass-**epoxy** , flexible Printed Circuit Board, and MCM-L/D). In this technology, Au bumps are formed on the chip I/O pads by **wire bonding** method, and the **bumps** are pressed against the **substrate** pads. The chip is bonded and encapsuled with a thermosetting adhesive, and conductive paste assists mechanical and electrical connection between the Au bumps and the **substrate** in order to increase the connection reliability. To apply this technology to different types of **substrates** , we surveyed the deformation characteristic of the **substrate** pad and the characteristic of the adhesive for **encapsulation** (adhesion strength and **insulation**).
This technology has been applied to some practical products and the mounting areas of LSI become 1/10 or less compared with existing SMD package approach.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

12/06/2002 09/992,387

73/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6264468 INSPEC Abstract Number: B1999-07-0170J-055
Title: Glob top plastic **ball grid array** package **encapsulation** process development and its moisture sensitivity study
Author(s): Yang, L.Y.; Padrinao, E.; Mui, Y.C.
Author Affiliation: Adv. Micro Devices, Singapore
Journal: International Journal of Microcircuits and Electronic Packaging vol.21, no.3 p.262-73
Publisher: IMAPS-Int. Microelectron. & Packaging Soc,
Publication Date: 1998 Country of Publication: USA
CODEN: IMEPE5 ISSN: 1063-1674
SICI: 1063-1674(1998)21:3L.262:GPBG;1-O
Material Identity Number: P802-1999-003
Language: English
Abstract: In glob top PBGA **encapsulation** process development, a design of experiments (DOE) is conducted to select critical process factors, and the response surface methodology (RSM) is used to optimize the process parameters. SPC tools are used to monitor process parameters and assess process capability. PBGAs have a high moisture absorption rate in a humid ambient, so moisture sensitivity is a concern when plastic packages are exposured to a humid environment and are then reflow processed. The moisture sensitivity study aims to assess moisture ingress effects on process and assembly reliability, using the steam pressure pot test, level-3 preconditioning test and temperature cycling test. Test results show that the substrate moisture content affects the die attach void level and size. The moisture level plays a part in die/substrate and **encapsulation** /substrate interface delamination after accelerated testing, but there is no correlation between die top delamination and moisture absorbed during the level-3 preconditioning test. No delamination was found at the die attach area or die/substrate interface, even when the package was fully moisture saturated and was temperature cycled. Greater delamination occurs at the molding compound/solder mask interface after steam pressure testing if more moisture is absorbed. Finally, plasma cleaning is found to have a significant effect on package integrity for dry packed PBGA and moisture saturated **units**. **Coupled** with the stress test results, it implies that the most important thing in PBGA assembly after moisture prevention is to enhance interface adhesion via plasma cleaning.

12/06/2002 09/992,387

75/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04073880
E.I. No: EIP95022579601
Title: UV curable urethane encapsulant for ceramic chip carriers
Author: Wilson, James W.
Corporate Source: IBM Microelectronics, Endicott, NY, USA
Source: IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A v 17 n 4 Dec 1994. p 553-558
Publication Year: 1994
CODEN: IMTAEZ ISSN: 1070-9886
Language: English
Abstract: A new acrylated urethane encapsulant has been formulated for use on ceramic chip carriers. This encapsulant has been implemented on **pin grid array** (PGA) ceramic carriers and on peripheral leaded surface mount (SMT) ceramic carriers for IBM's C4 chips. The encapsulant is a UV curable material and is used to cover the thin film circuitry on the ceramic carrier. The encapsulant offers a low cost alternative to metal caps that are used on PGA ceramic carriers or to the ceramic cap that was used on the peripheral leaded surface mount carrier. 8

77/3,AB/1 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01825165 AADAAI3006904
Assembly and reliability of lead-free flip chips
Author: Tonapi, Sandeep Shrikant
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: State University of New York at Binghamton (0792)
Source: VOLUME 62/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1556. 192 PAGES
ISBN: 0-493-16230-5

The small dimensions and the integrated layer structure of a typical underfilled flip chip assembly lead to some rather unique concerns in terms of process windows, assembly yields, and reliability. In driving towards no-Pb soldering, it is important to keep all of these and the consequences for design, materials selection and process optimization in mind. Experimental results for **Ball Grid Array** (**BGA**) or SMT components are not readily applicable for flip chips.

This dissertation focuses on understanding the soldering phenomenon for leadfree flip chips. First, the potential lead-free solder alternatives were identified for flip chip applications. Four selected alloys were evaluated for wetting and solder joint collapse under two substantially different conditions, soldering to a blanket Organic Solder Protect (OSP) coated copper surface and to individual **contact pads** on substrates designed to match the die, respectively. Based on the results from these experiments, the 95.5Sn/3.5Ag/1.0Cu (LF-2) soldering system was considered for a detailed investigation.

LF-2 solder joints reflowed quite readily at moderate peak temperatures and time above the liquidus temperature. Minimum temperatures and times shown to give full collapse were 238°C and 40 seconds when the bumps were dipped in a 2 mil thick film of flux. Unfortunately, wetting and collapse rapidly became sensitive to flux thicknesses below 2 mils, i.e. the process window is narrow. Solder wetting and collapse did not depend on the flux type (for the fluxes considered). Almost complete collapse was achieved on OSP coated copper pads whereas the Sn/Ag/Cu solder does not collapse completely when placed onto Ni/Au pads.

Even though reflow parameters did not affect solder joint collapse, there was a significant difference in the solder joint properties for different reflow parameters. These differences in the solder joint properties resulted in a difference in the mechanical strength of the solder joint. The fatigue resistance of both, **encapsulated** and non-**encapsulated** LF-2 joints was significantly lower on Ni/Au-pads than on Cu/OSP. There was faster failure with slower delamination for the assemblies on Ni/Au pads when solder fatigue was the dominant failure mechanism. Local adhesion of the underfill to the chip passivation and the solder surface was dependent on the combination of the flux, the underfill material, the solder alloy and the substrate pad metallurgy. Thermal shock testing of underfilled LF-2 assemblies showed good performance when the thickness of the encapsulant fillet was properly controlled. Very thick and very thin fillets resulted in corner delamination and immediate failure

when the delamination reached the solder joints. Fatigue failures were observed when the thickness of the encapsulant fillet was controlled to delay/eliminate corner delamination.

12/06/2002 09/992,387

77/3,AB/2 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15043946 PASCAL No.: 01-0201455
Wafer level packaging of a tape flip-chip chip scale packages
HOTCHKISS G; AMADOR G; EDWARDS D; HUNDT P; STARK L; STIERMAN R; HEINEN G
Texas Instruments Incorporated MS 940, Dallas, TX 75265, United States
Journal: Microelectronics and Reliability, 2001, 41 (5) 705-713
Language: English
The advent of chip scale packages (CSPs) within the semiconductor community has led to the development of wafer scale assembly (WSA) or wafer level packaging (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip-chip, **ball grid array** packages. The die inputs and outputs of the TI CSP are connected through solder bumps to a polyimide film interposer. Solder balls on the other side of the interposer complete the electrical connection to a customer's printed circuit board. A wafer-sized array of interposers designed to match the pattern of dies on a wafer is aligned and reflowed to a bumped wafer. The TI WLP process is completed by singulating the CSPs from the wafer using standard wafer saw equipment. Attachment of the interposer to the die as well as applying the die and board level solder bumps are carried out in wafer form using a new bumping technology called Tacky Dots Degree trademark<pilcrow>. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a polyimide film for transferring and attaching solder spheres to semiconductor substrates. A populated film containing one solder sphere per Tacky Dot is positioned over the wafer or interposer and lowered until the spheres **contact** the **pads**. A reflow process transfers the spheres from the film to the wafer or interposer and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the package is outlined. The paper concludes by summarizing the current package level reliability results. (c) 2001 Elsevier Science Ltd.

12/06/2002 09/992,387

82/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6887165 INSPEC Abstract Number: B2001-05-0170J-143
Title: **Copper bump** bonding with electroless metal cap on 3 dimensional stacked structure
Author(s): Tomita, Y.; Tago, M.; Nemoto, Y.; Takahashi, K.
Author Affiliation: Electron. Syst. Integration Technol. Res. Dept., Tsukuba Res. Center, Ibaraki, Japan
Conference Title: Proceedings of 3rd Electronics Packaging Technology Conference (EPTC 2000) (Cat. No.00EX456) p.286-91
Editor(s): Beng, L.T.; Lee, C.; Chuan, T.K.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 467 pp.
ISBN: 0 7803 6644 1 Material Identity Number: XX-2000-03026
U.S. Copyright Clearance Center Code: 0 7803 6644 1/2000/$10.00
Conference Title: Proceedings of 3rd Electronics Packaging Technology Conference
Conference Sponsor: IEEE CPMT Soc.; IMAPS; ASME; Ginitic Inst. Manuf. Technol.; Inst. Mater. Res. & Eng.; Inst. Microelectron.; Nanyang Technol. Univ.; Nat. Univ. Singapore
Conference Date: 5-7 Dec. 2000 Conference Location: Singapore
Language: English
Abstract: CBB, the **copper bump** bonding process, can perform **flip-chip** bonding in **100 mu** m **pitch** with a thin electroless metal cap on the surface, leading to interconnection of the copper through-hole electrodes on a 3D stacked structure. In this paper, the results of the technical studies on both the electroless plating process and the thermo-compressive bonding process are introduced, which are key technologies for expansion to interconnections with 20 **mu** m **pitch** to realize advanced 3D stacked structures.

82/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6551485 INSPEC Abstract Number: B2000-05-0170J-043, C2000-05-3350E-007
Title: Process control of high density solder bumps by electroplating technology
Author(s): Szu-Wei Lu; Zhao-Hui Wu; Yuh-Jiau Huang; Ruoh-Huey Uang; Wei-Chung Lo; Hsu-Tien Hu; Yu-Fang Chen; Ling-Chen Kung; Hsin-Chien Huang
Author Affiliation: Packaging Process Dept., Ind. Technol. Res. Inst., Hsinchu, Taiwan
Conference Title: Twenty Fourth IEEE/CPMT International Electronics Manufacturing Technology Symposium (Cat. No.99CH36330) p.325-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xiv+479 pp.
ISBN: 0 7803 5502 4 Material Identity Number: XX-1999-02924
U.S. Copyright Clearance Center Code: 0 7803 5502 4/99/$10.00
Conference Title: Twenty Fourth IEEE/CPMT International Electronics Manufacturing Technology Symposium
Conference Sponsor: IEEE; Semicond. Equipment and Mater. Int
Conference Date: 18-19 Oct. 1999 Conference Location: Austin, TX, USA
Language: English
Abstract: In this paper, we describe the process control of high-density solder bumps by electroplating with high uniformity and repeatability. The die size is 10*10 mm and it has 1,520 total I/Os. The electroplated bump is composed of eutectic Sn/Pb with a **pitch** of 250 **mu** m and height of **100** **mu** m. Ti/Cu is used as the UBM (under bump metallurgy) which is deposited by sole sputtering. The nonuniformity of the bump heights is found to be less than 5% in a 6" wafer. The PR (photoresist) opening is 101+or-1 mu m within wafers and 101+or-2 mu m wafer-to-wafer. The deviation of the PR thickness is within +or-2 mu m for a typical thickness of 45. The alignment accuracy is better than 1.5 mu m. The shear force of the UBM as sputtered is comparable to that incorporated with electroplated Cu reported in the literature. The reliability is investigated for different Cu thicknesses. The reliability test of high temperature storage at 150 degrees C shows that shear force remains constant for more than 650 hours and drops to one half of the original value after 2,000 hours for a 4 mu m sputtering Cu UBM. It is also found that the shear force does not decay after ten reflow cycles.

12/06/2002 09/992,387

85/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7116248 INSPEC Abstract Number: B2002-01-2240-011
Title: Under bump metallisation of fine pitch **flip-chip** using electroless nickel deposition
Author(s): Liu, C.; Hutt, D.A.; Whalley, D.C.; Conway, P.P.; Mannan, S.H.
Author Affiliation: Wolfson Sch. of Mech. & Manuf. Eng., Loughborough Univ. of Technol., UK
Journal: Journal of Electronics Manufacturing vol.10, no.3 p.161-70
Publisher: World Scientific,
Publication Date: Sept. 2000 Country of Publication: Singapore
CODEN: JELMEK ISSN: 0960-3131
SICI: 0960-3131(200009)10:3L.161:UBMF;1-3
Material Identity Number: F164-2001-003
Language: English
Abstract: For solder based **flip-chip** assembly, the deposition of an under bump metallisation (UBM) layer onto the surface of the Al bondpads of the die is the first step in the wafer bumping process. The UBM is necessary, as the fragile Al pad has a tenacious oxide layer that cannot be soldered without the use of strong fluxes and a barrier layer is required to prevent dissolution of the bondpad into the solder during reflow. The requirements of the UBM are therefore to provide a solder wettable surface and to protect the underlying Al bondpad during and after assembly. In addition, the UBM deposition process itself must remove any oxide layers on the bondpads to ensure a low resistance interface between the pad and the UBM. This paper reports an investigation of the electroless **nickel** deposition process for the under **bump** metallisation of wafers that are subsequently to be bumped using solder paste printing. In particular this work has extended the process from previous trials on 225 **mu** m **pitch** devices to wafers including die with sub **100** **mu** m **pitch** bondpads. As part of this work, the effect of the various pre-treatment etching processes and zincate activation on the quality of the final electroless **nickel** **bump** has been investigated. The use of SEM examination of samples at each stage of the bumping process has been used to aid a detailed understanding of the activation mechanisms and to determine their effects on the electroless **nickel bump** morphology. In addition, shear testing of bumps has been used to determine the best pre-treatment regime to ensure good adhesion of the electroless nickel to the bondpad. Finally, electrical resistance measurements of bumped die have been used to confirm that the pre-treatment procedures are producing a low resistance interface between the Al and electroless nickel.

12/06/2002 09/992,387

85/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6880896 INSPEC Abstract Number: B2001-05-2240-011
Title: Influences of pad shape and solder microstructure on shear force of low cost **flip chip** bumps
Author(s): Jian Cai; Law, S.; Teng, A.; Chan, P.C.H.
Author Affiliation: Computer Aided Design & Manuf. Facility, Hong Kong Univ. of Sci. & Technol., China
Conference Title: International Symposium on Electronic Materials and Packaging (EMAP2000) (Cat. No.00EX458) p.91-8
Editor(s): Kim, J.K.; Teng, A.; Lee, S-W R.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xii+478 pp.
ISBN: 0 7803 6654 9 Material Identity Number: XX-2001-00192
U.S. Copyright Clearance Center Code: 0 7803 6654 9/2000/$10.00
Conference Title: International Symposium on Electronic Materials and Packaging (EMAP2000)
Conference Sponsor: Adv. Interconnect Technol.; ASM Pacific Technol.; ASME Int. - Hong Kong Sect.; Compass Technol. Co.; US Army Res. Office - Far East; Inst. Mater. Res. & Eng. (IMRE), Singapore; Nanyang Technol. Univ. Singapore
Conference Date: 30 Nov.-2 Dec. 2000 Conference Location: Hong Kong, China
Language: English
Abstract: The bumping process plays a critical role in **flip chip** technology. A low cost bumping process has been developed using electroless nickel and immersion gold followed by stencil printing. The process flow is described in this paper. The Al pad size is about **100 mu** m in diameter with a **pitch** of 400 **mu** m. Different electroless plating solutions were evaluated and different solder pastes were used to evaluate the stencil printing process. Different pad shapes were also tested for shear strength. **Ni** studs with no **bump** material were fabricated to evaluate the electroless process. The shear force test result shows a strength value of 230 MPa for **Ni** studs. The solder **bump** after reflow has a diameter of 160 mu m and a height of 120 mu m. There is some difference in the shear force test results for different pad shapes. SEM and EDAX results of the fracture surface indicate that the fracture was cohesive or inside the solder. Cross sections showed some intermetallic layers at the interface. A Ni-Sn intermetallic layer and a phosphorus rich layer formed during reflow, which have compositions of Ni/sub 3/Sn/sub 4/ and Ni/sub 3/P respectively. The low cost **flip chip** samples were subjected to multiple reflows and shear force tests were performed. Fracture surfaces were analysed and failure modes were differentiated.

85/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6383857 INSPEC Abstract Number: B1999-12-0170J-006
Title: Development of 0.025 mm pitch anisotropic conductive film
Author(s): Eriguchi, F.; Maeda, M.; Asai, F.; Hotta, Y.
Author Affiliation: Center of Core Technol., Nitto Denko Corp., Osaka, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3582 p.219-23
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3582L.219:D0PA;1-H
Material Identity Number: C574-1999-173
Conference Title: 1998 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS
Conference Date: 1-4 Nov. 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: Anisotropic conducting adhesive technology for **flip chip** interconnection is being actively investigated in the electronics industry at present. We are developing a novel anisotropic conductive film (ACF) which can connect a bump-less chip and a high density printed wiring board (PWB). This ACF is composed of linear metal material "pillars" (not small conductive particles) and thermoplastic polymer resin. This **flip-chip** interconnection with the ACF between **bump** -less chip pads and **Ni**/Au plated pads (**100 mu** m **pitch**) on an FR-4 PWB shows good reliability in various environmental tests such as thermal cycling tests (-50 degrees C/+125 degrees C, 1000 cycles), pressure cooker tests (120 degrees C, 2.1 atm, 100% RH, 144 hr) and temperature humidity bias tests (85 degrees C, 85% RH, 5.5 V, 1000 hr).

87/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6455656 INSPEC Abstract Number: B2000-02-2240-006
Title: Single chip bumping and reliability for **flip chip** processes
Author(s): Klein, M.; Oppermann, H.; Kalicki, R.; Aschenbrenner, R.; Reichl, H.
Author Affiliation: Center of Microperipheric Technol., Tech. Univ. Berlin, Germany
Journal: Microelectronics Reliability vol.39, no.9 p.1389-97
Publisher: Elsevier,
Publication Date: Sept. 1999 Country of Publication: UK
CODEN: MCRLAS ISSN: 0026-2714
SICI: 0026-2714(199909)39:9L.1389:SCBR;1-3
Material Identity Number: G489-1999-008
U.S. Copyright Clearance Center Code: 0026-2714/99/$20.00
Language: English
Abstract: The processes of bump deposition based on mechanical procedures together with their reliability data are summarized in this paper. The stud bumping of gold, palladium, and solder is described and also a novel bumping approach for fine pitch solder deposition down to **100 mu** m **pitches** using thermosonic bonding on a modified wedge-wedge bonding machine. This wedge bumping does not require a wire flame-off process step. Because of this, no active atmosphere is necessary. The minimum pad diameter which can be bumped using the solder wedge bumping is 50 mu m, up to now. This bumping process is highly reproducible and therefore well-suited for different **flip chip** soldering applications. **Palladium** stud **bumps** provide a solderable under bump metallization. Results from aging of lead/tin solder **bumps** on **palladium** are shown. The growth of intermetallics and its impact on the mechanical reliability are investigated.

12/06/2002 09/992,387

89/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6405909 INSPEC Abstract Number: B1999-12-2240-019
Title: Development and applications of stud-bump bonding technology
Author(s): Bessho, Y.; Omoya, K.; Ohbayashi, T.
Journal: Matsushita Technical Journal vol.45, no.4 p.3-11
Publisher: Matsushita Electric Industrial Co,
Publication Date: Aug. 1999 Country of Publication: Japan
ISSN: 1343-9529
SICI: 1343-9529(199908)45:4L.3:DASB;1-R
Material Identity Number: G497-1999-005
Language: Japanese
Abstract: **Flip-chip** mounting technology has been developed using the stud-bump bonding (SBB) method which directly mounts a bare LSI chip on the circuit board. This method uses two-stage shaped projection electrodes and conductive adhesive, making possible fine connection at less than **100 mu** m **pitch** . For securing reliability of the mounting, it is important to optimize the conductive adhesive and underfill material. For this purpose, a high-molecular-weight thermoplastic **resin** with flexibility over a wide temperature range, and a conductive adhesive using conductive filler have been developed. Also, underfill material has been developed using a filler with optimized grain-size distribution and a **resin** material with low-viscosity, high-adhesive-strength and low-moisture-absorption. Thereby the connection between the LSI chip and circuit board is stabilized. Thus, LSI chips can be mounted with high reliability on various kinds of circuit boards, such as glass, ceramic and glass-**epoxy**, making possible application to MCM, CSP, etc.

89/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6383857 INSPEC Abstract Number: B1999-12-0170J-006
Title: Development of 0.025 mm pitch anisotropic conductive film
Author(s): Eriguchi, F.; Maeda, M.; Asai, F.; Hotta, Y.
Author Affiliation: Center of Core Technol., Nitto Denko Corp., Osaka, Japan
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3582 p.219-23
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3582L.219:DOPA;1-H
Material Identity Number: C574-1999-173
Conference Title: 1998 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS
Conference Date: 1-4 Nov. 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: Anisotropic conducting adhesive technology for **flip chip** interconnection is being actively investigated in the electronics industry at present. We are developing a novel anisotropic conductive film (ACF) which can connect a bump-less chip and a high density printed wiring board (PWB). This ACF is composed of linear metal material "pillars" (not small conductive particles) and thermoplastic polymer **resin**. This **flip-chip** interconnection with the ACF between bump-less chip pads and Ni/Au plated pads (**100 mu** m **pitch**) on an FR-4 PWB shows good reliability in various environmental tests such as thermal cycling tests (-50 degrees C/+125 degrees C, 1000 cycles), pressure cooker tests (120 degrees C, 2.1 atm, 100% RH, 144 hr) and temperature humidity bias tests (85 degrees C, 85% RH, 5.5 V, 1000 hr).

12/06/2002 09/992,387

89/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5709620 INSPEC Abstract Number: B9711-2250-014
Title: Development of fluxless **flip chip** bonding to a thin film multichip module substrate
Author(s): Bonda, R.; Fang, T.; Hileman, B.; Spigler, D.; Stafford, J.; Swan, G.; Tam, G.
Author Affiliation: Motorola Inc., Tempe, AZ, USA
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.875-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: Motorola SPS has developed an assembly process for a three-chip multichip module using a fluxless bonding technique. The substrate is a 25 mm*25 mm glass that containing two layers of electroplated metallization with vias connecting the two layers and dielectric layer separating them. A test substrate is designed to characterize the continuity and leakage of the assembled modules. One of the chips has two staggered rows of 384 total bumps on the periphery with 80 **mu** m **pitch** and 45 **mu** m bump size. The other two chips have three staggered rows, 222 bumps on each chip, 210 **mu** m **pitch** and **100 mu** m bump size. The bump composition is Pb-Sn with low Sn content. All three chips are bonded to the substrate using a fluxless plasma process followed by reflow in a nitrogen furnace. A high precision robot is used for placement and tacking of the chips on the substrate. After the bonding, the chips are underfilled with a proprietary underfill **epoxy**, and tested for reliability. All the reliability criteria for the specific application of this module have been met. Physical design and assembly process of this multichip module will be presented.

12/06/2002 09/992,387

89/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5565268 INSPEC Abstract Number: B9706-0170J-018
Title: Plastic LGA889 using **flip-chip** bonding on build-up substrate
Author(s): Minamizawa, M.; Iijima, M.; Ueno, S.; Akai, T.; Nukiwa, M.; Ihara, T.; Hamano, T.; Soekawa, K.; Miyazawa, Y.; Shirotsuki, T.
Author Affiliation: ASIC Packaging Eng. Dept., Fujitsu Labs. Ltd., Kawasaki, Japan
Conference Title: Proceedings. 1996 International Symposium on Microelectronics (SPIE Vol.2920) p.271-8
Publisher: Microelectron. Soc, Reston, VA, USA
Publication Date: 1996 Country of Publication: USA xiii+610 pp.
ISBN: 0 930815 48 3 Material Identity Number: XX96-03083
Conference Title: 1996 International Symposium on Microelectronics
Conference Sponsor: Microelectron. Soc
Conference Date: 8-10 Oct. 1996 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: Process development work was undertaken to achieve advanced high density and high performance packaging for 0.35 mu m CMOS ASICs. The clock frequency of the device is 134 MHz, there are 200 simultaneous switching outputs, and heat dissipation is 20 watts. To accommodate this high integration and high performance device, we newly developed a build-up substrate and **flip-chip** bonding technology. The organic build-up substrate has excellent routability. By using photosensitive **epoxy** dielectric, fine staggered vias can be formed, and by using electrodeposited etching resist, fine patterns can be routed. A triple build-up layer is laminated on both the top and the bottom of a 6-layer subtractive printed wiring board. The diameter of the photosensitive via is **100 mu** m, and the minimum line width and space are 45 mu m each. The **flip-chip** bonding is accomplished at low temperature to the organic substrate between the 95 Pb/Sn solder bump and pre-reflowed solder Sn-Ag alloy. The bump has an area-array configuration with 245 **mu** m **pitch**. Underfill **resin** is filled under the device to decrease CTE mismatch. The package has 889 land-counts in a 1.27 mm land pitch. The package size is 42.5 mm*42.5 mm. This paper addresses the design, process flow, electrical and thermal characteristics and excellent reliability test results of the package.

12/06/2002 09/992,387

89/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04067320 INSPEC Abstract Number: B9202-2220J-024
Title: Chip attach for silicon hybrid multi-chip modules
Author(s): Collier, P.A.
Author Affiliation: STC Technol. Ltd., Harlow, UK
Conference Title: 8th IEMT 1990. International Electronic Manufacturing Technology Symposium (Cat. No.90CH2833-2) p.53-62
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA viii+515 pp.
U.S. Copyright Clearance Center Code: CH2833-2/90/0000-0053$01.00
Conference Sponsor: IEEE
Conference Date: 7-9 May 1990 Conference Location: Baveno, Italy
Language: English
Abstract: The author describes the requirements of chip attachment techniques for silicon hybrid circuits, compares **flip-chip**, tape automated bonding (TAB), and wire bonding, and discusses the significance of assembly yield and test. Although area array **flip-chip** technology provides perhaps the ultimate electrical interconnection density, TAB can also be applied in very-high-density format. Silicon devices can be bonded face down with short beam leads and equal inner and outer lead-bonding (OLB) pitches. Assembly of high-lead-count TAB test chips onto fine-line aluminum-**polyimide** and copper-**polyimide** connections on silicon substrates has been evaluated in the RISH (Research Initiative into Silicon Hybrids) program. A range of bonding experiments was completed. Solder assembly was achieved with box thermode reflow down to OLB **pitches** of 175 **mu** m, with possible extension to bonding at 125 mu m or less. Single-point gold-gold OLB was achieved at **100- mu** m bond **pitches**.

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89/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04819479
E.I. No: EIP97093821998
Title: Development of low cost and reliable **resin** based PRESS CONTACT technology
Author: Yoshino, Rieka; Murakami, Tomoo; Tanaka, Kei; Shimada, Toshiyasu
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1997 IEEE/CPMT 20th International Electronic Manufacturing Symposium
Conference Location: Tokyo, Jpn Conference Date: 19970416-19970418
E.I. Conference No.: 46958
Source: Proceedings of the IEEE/CPMT International Electronic Manufacturing Technology (IEMT) Symposium 1997. IEEE, Piscataway, NJ, USA,97CH36059. p 158-163
Publication Year: 1997
CODEN: 61UNAI
Language: English
Abstract: We have developed a new **flip chip** assembly method, PRESS CONTACT technology, without the connective material supplying. This flow: first, dropping **epoxy resin** at the center of the LSI mount area on the PWB. Next, positioning bump of LSI electrode toward pad of PWB, and attaching under designed temperature and pressure. As a result, hardening the **epoxy resin** by this process, the simple process is all over. The **resin** of this method have no conductive particles as the connective material, and hold the attachment between LSI and PWB by the only force of **resin** shrinkage, and can maintain the contacting connection between LSI bump and PWB pad, too. In reliability evaluation of the PRESS CONTACT technology using **resin,** the endurance of the contacts exceeded 700 cycles of thermal cycling test (minus 40 DGR@C-125 degree C) and 400 hrs of pressure cooker test (110 degree C, 85% RH). The PRESS CONTACT technology will be positioned as one of the **flip chip** assembly. And we will proceed with the improvement of the reliability and the development of the very fine pad pitch level (less than **100 microns pitch**). (Author abstract) 3 Re

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89/3,AB/7 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04171790 JICST ACCESSION NUMBER: 99A0718519 FILE SEGMENT: JICST-E
High-Density Mounting Technologies. Development and Applications of Stud-Bump Bonding Technology.
BESSHO YOSHIHIRO (1); OMOYA KAZUNORI (2); OBAYASHI TAKASHI (2)
(1) Matsushita Electric Industrial Co., Ltd., JPN; (2) Matsushita Technoresearch, Inc.
Matsushita Tech J, 1999, VOL.45,NO.4, PAGE.365-373, FIG.14, TBL.3, REF.11
JOURNAL NUMBER: G0474ABY ISSN NO: 1343-9529
UNIVERSAL DECIMAL CLASSIFICATION: 621.3.049.75
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: **Flip-chip** mounting technology has been developed using the Stud-Bump Bonding(SBB) method which directly mounts a bare LSI chip on the circuit board. This method uses 2-stage shaped projection electrodes and conductive adhesive, making possible fine connection at less than **100.MU**.m **pitch**. For securing reliability of the mounting, it is important to optimize the conductive adhesive and under-fill material. For this purpose, a high-molecular-weight thermoplastic **resin** with flexibility over a wide temperature range, and a conductive adhesive using conductive filler have been developed. Also, under-fill material has been developed using a filler wiht optimized grain-size distribution and a **resin** material with low-viscosity, high-adhesive-strength and low-moisture-absorption. Thereby the connection between the LSI chip and circuit board is stabilized. Thus, LSI chips can be mounted with high reliability on various kinds of circuit boards, such as glass, ceramic and glass-**epoxy**, making possible application to MCM, CSP, etc. (author abst.)

12/06/2002 09/992,387

93/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04526493
E.I. No: EIP96043156589
Title: Optoelectronic ATM switch employing hybrid **silicon** CMOS/GaAs FET-SEEDs
Author: Lentine, Anthony L.; Reiley, Daniel J.; Novotny, Robert A.; Morrison, Rick L.; Sasian, Jose M.; Beckman, Martin G.; Buchholz, D.B.; Hinterlong, Stephen J.; Cloonan, Thomas J.; Richards, Gaylord W.; McCormick, Frederick B. Jr.
Corporate Source: AT&T Bell Labs., Naperville, IL, USA
Conference Title: Optical Interconnects in Broadband Switching Architectures
Conference Location: San Jose, CA, USA Conference Date: 19960131-19960201
E.I. Conference No.: 22515
Source: Proceedings of SPIE - The International Society for Optical Engineering v 2692 1996. Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, USA. p 100-108
Publication Year: 1996
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-2066-2
Language: English
Abstract: In the past few years, the demand for telecommunications services beyond voice telephony has skyrocketed. For the growth of these services to continue at this rate, cost effective means of transporting and switching large amounts of information must be found. Although fiber optic transmission has significantly reduced the cost of transmission, switching high bandwidth signals remains expensive. While all electronic switching systems are certainly possible for these high bandwidth systems, considerable effort has been expended to reduce the cost of fiber optic connections between frames or racks of equipment separated by several meters. As an example, one can envision fiber-optic data **links connecting** the line **units** that receive and transmit data from the outside world with an electronic switching fabric. Optical data links, ODLs, can perform the optical to **electrical** conversions. Several of these optical data links can be electrically connected with electronic switching chips on a printed circuit board. As the demand for bandwidth increases, several hundred to several thousand optical fibers might be incident on the switching fabric. Discrete optical data links and parallel data links with up to 32 fibers per data link remain an expensive solution to transporting this information due to their per-link cost, physical size, and power dissipation. Power dissipation on the switching chips is high because of the need for electronic drivers for the high speed **electrical** interconnections between the switching chips and the data links. By integrating the O/E conversions directly onto the switching chips, lower cost and higher density systems can be built. In this paper, we describe preliminary results of an experimental optoelectronic switching network based on this lower cost solution. The network is designed to be part of an asynchronous transfer mode (ATM) network based on the Growable Packet Architecture. The switching chip consists of GaAs/AlGaAs multiple quantum well modulators and detectors **flip- chip** bonded to **silicon** VLSI circuitry. The optical system images the inputs from a two dimensional fiber bundle onto the switching chip, provides optical

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97/3,AB/1 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15043946 PASCAL No.: 01-0201455
Wafer level packaging of a tape flip-chip chip scale packages
HOTCHKISS G; AMADOR G; EDWARDS D; HUNDT P; STARK L; STIERMAN R; HEINEN G
Texas Instruments Incorporated MS 940, Dallas, TX 75265, United States
Journal: Microelectronics and Reliability, 2001, 41 (5) 705-713
Language: English
The advent of chip scale packages (CSPs) within the semiconductor community has led to the development of wafer scale assembly (WSA) or wafer level packaging (WLP) manufacturing in order to raise assembly efficiencies and lower operating costs. Texas Instruments (TI) has developed a unique WLP process for forming flip-chip, **ball grid array** packages. The die inputs and outputs of the TI CSP are connected through solder bumps to a **polyimide** film interposer. Solder balls on the other side of the interposer complete the electrical connection to a customer's printed circuit board. A wafer-sized array of interposers designed to match the pattern of dies on a wafer is aligned and reflowed to a bumped wafer. The TI WLP process is completed by singulating the CSPs from the wafer using standard wafer saw equipment. Attachment of the interposer to the die as well as applying the die and board level solder bumps are carried out in wafer form using a new bumping technology called Tacky Dots Degree trademark<pilcrow>. Tacky Dots uses an array of sticky dots formed in a photosensitive coating laminated to a **polyimide** film for transferring and attaching solder spheres to semiconductor substrates. A populated film containing one solder sphere per Tacky Dot is positioned over the wafer or interposer and lowered until the spheres **contact** the **pads** . A reflow process transfers the spheres from the film to the wafer or interposer and the film is removed once the spheres have frozen. This paper illustrates the process steps and custom equipment developed for forming the TI CSP. The strategic use of finite element modeling for optimizing the design of the package is outlined. The paper concludes by summarizing the current package level reliability results. (c) 2001 Elsevier Science Ltd.

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99/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03955356 JICST ACCESSION NUMBER: 99A0180831 FILE SEGMENT: JICST-E
Development of **Coated-Wire Bonding** Technology.
KANEDA TSUYOSHI (1); WATANABE HIROSHI (2); AKIYAMA YUKIHARU (2); TSUBOSAKI KUNIHIRO (2); NISHIMURA ASAO (2); NISHI KUNIHIKO (2)
(1) Hitachi Micrcomputer System Ltd.; (2) Hitachi, Ltd.
Yosetsu Gakkai Ronbunshu(Quarterly Journal of the Japan Welding Society), 1998, VOL.16,NO.4, PAGE.540-547, FIG.10, TBL.4, REF.7
JOURNAL NUMBER: Y0413AAA ISSN NO: 0288-4771
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: **Wire bonding** technology is being applied to narrower pad piches and longer spans in LSI packages with the increase in number of input-output pins and shrinkage in chip size. This makes adjoining wires liable to touch during the molding process. To solve fundamentally this problem, the authors have been developing bonding technologies, using **coated** gold wires which do not suffer from short circuit failures even if the wire touch occurs. In this study, various **coated** wires were evaluated to select the optimum **coating** film with improved resistance to the wire touch at high tempratures and improved bonding continuity. Packages were then assembled with the selected wires, and various reliability tests were conducted. The best properties were obtained with the **coating** film of 0.4.MU.m thick heat-resistant formal, which showed high **insulation** reliability in a high temperature wire-crossing test and enabled continual bonding for more than one hundred thousand wire connections. It was confirmed that the assembled packages have sufficient **insulation** reliability between touching wires and that no failures occurred in various reliability tests including temperature cycling and high temperature high humidity bias tests. (author abst.)

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99/3,AB/2 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03377766 JICST ACCESSION NUMBER: 97A0629150 FILE SEGMENT: JICST-E
Semiconductor device.
HORI TETSUJI (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1997, VOL.15,NO.39, PAGE.111-114, FIG.6
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: By executing a **wire bonding** afte **connecting** a power circuit **part** formed on an **insulation** heat radiation **substrate** and a control circuit part such as a thick film **substrate** to a metal frame, a mounting method which the resin molding could be adopted for the circumference was devised. Because a metal-**based substrate** and an insert molding resin case can be decreased, the cost reduction and miniaturization are made possible.

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102/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5920125 INSPEC Abstract Number: B9806-0170J-058
Title: Adhesive flip chip bonding on flexible substrates
Author(s): Aschenbrenner, R.; Miessner, R.; Reichl, H.
Author Affiliation: Fraunhofer Inst. fur Zuverlassigkeit und Mikrointegration, Berlin, Germany
Conference Title: Proceedings. The First IEEE International Symposium on Polymeric Electronics Packaging, PEP '97 (Cat. No.97TH8268) p.86-94
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 333 pp.
ISBN: 0 7803 3865 0 Material Identity Number: XX98-00536
U.S. Copyright Clearance Center Code: 0 7803 3865 0/97/$8.00
Conference Title: Proceedings. The First IEEE International Symposium on Polymeric Electronics Packaging, PEP '97 (Cat. No.97TH8268)
Conference Sponsor: Ericsson; NUTEK; City of Norrkoping
Conference Date: 26-30 Oct. 1997 Conference Location: Norrkoping, Sweden
Language: English
Abstract: Flip chip attach provides the highest interconnection density possible, making this technology attractive for use with high density flex substrates. This paper presents three approaches to a flip chip adhesive process based on flexible polyimide and polyester substrates using Au, **Ni**-Au and Au stud **bumps** with anisotropic adhesives, isotropic conductive adhesives and nonconductive adhesives. Isotropic conductive adhesives conduct equally in all directions. For flip chip application of such adhesives, the material must be applied precisely on the points to be electrically connected and not allowed to flow and short circuit between circuit lines. Anisotropically conductive adhesives are prepared by dispersing conductive particles in an adhesive matrix at high enough concentration to assure reliable conductivity between substrate and IC electrodes. Another possibility is the use of nonconductive adhesives and Au-bumped chips, which are bonded via thermocompression to the substrate. During **bonding**, the **bumps** pierce a nonconducting adhesive foil and make electrical contact while the adhesive supplies mechanical stability. Moreover, the adhesive fills the gap between chip and substrate, relieving the bumps of mechanical stress due to the different CTEs. Reliability evaluation was performed with specific regard to the interface reactions between polymers and metal surfaces in adhesive contacts. The electrical and mechanical performance of the adhesive bonds were studied by evaluating initial contact resistance as a function of temperature and humidity.

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102/3,AB/2 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

13244255 PASCAL No.: 97-0514034
High-performance Cavity-Down Metal Based Ball Grid Array (MeBGA) package
SUZUKI K; SORIMACHI I; UCHIDA H; SHIBUYA K; HAGA A
C&C LSI Development Division, Japan; VLSI Packaging and Testing Engineering Division, Japan
Journal: NEC research & development, 1997, 38 (3) 306-317
Language: English
The recent trend in microprocessor technology is for high-speed devices (200 similar 500 MHz) on which a large number of drivers simultaneously switch on/off. On the other hand, the trend in high-performance ASIC devices is also for higher on- and off-chip devices speed; higher chip I/O density; and larger power. Our newly developed high-performance Cavity-Down (C/D) Metal Based Ball Grid Array (MeBGA) package is constructed of a unique three-layer substrate, which is composed of a copper foil and copper alloy substrate which are **insulated** with polyimide. The MeBGA has two unique and important structures, which are terminal and ground bonding area. As a result, MeBGA realizes higher thermal performance, higher electrical performance and lower cost than those of conventiunal Plastic BGA (PBGA). For example, thermal resistance is 40% lower than that of conventional PBGA package at 1.0 m/s air velocity. Electrical analysis is presented to show that the simultaneous switching noise including the ground bounce noise and power supply noise is about 40% lower than that of conventional PBGA. The terminal is fabricated on the rear side of MeBGA for currently testing interconnection between **solder balls** and the Printed Wiring Board (PWB), and also reducing the thermal expansion stress between **solder ball** and **copper** foil. The ground **bonding** area has a flat area fabricated around the slope of die cavity for direct wire bonding to the copper substrate. Both terminal and ground bonding areas are provided with a much simpler process. This paper describes MeBGA's structure, assembly process, some characteristics, and the results of a reliability test.